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EXAMINER	
COLEMAN, ERIC	

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2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/836,541	Applicant(s) KINTER ET AL.	
	Examiner Eric Coleman	**Art Unit** 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/16/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8,10-14 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,10-14 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required (Claim 10 is reciting computer program product. However no clear and deliberate definition of computer program product can be found in the specification.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 10-14, and 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As to claim 10-14, claim 10-14 recite computer program product comprising a tangible computer readable storage medium in the preamble. However, in view of the specification there is no clear definition that the computer readable storage medium is necessary in hardware Page 13, [0054] of the specification taught computer usable (e.g., readable) medium includes both hardware, CD ROM, DVD ROM and hardware as a computer data signal embodied in a computer usable transmission medium (e.g., see carrier wave). Therefore it is not necessarily in hardware.

As to claim 30, in claim 30 additionally recites the tangible computer readable storage medium includes at least one semiconductor disk, a magnetic disk and a optical disk. However, this is not limiting the claim scope because in view of the specification the computer readable storage is not excluding a computer data signal embodied in a

computer usable transmission medium (e.g., carrier wave). Suggested language is : the tangible computer readable storage medium consisting of at least one of semiconductor disk, a magnetic disk and a optical disk.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) in view of Overkamp (patent No. 7,069,420).

As to claim 31, Brennan taught a cache memory adapted to output a plurality of instructions, wherein each instruction is associated with one of the instruction sets; (a) cache controller having a parallel mapper to map each of the plurality of instructions into a predetermined instruction width format (not explicitly characterized as cache controller, but see how the prefetch instructions from the cache 30 in fig. 4, see also fig. 4 (35) see fig. 5 for details of the decoder as parallel mappers); (b) tag comparator to compare tage (see most significant bits) associated with each instruction in the plurality of instructions with a tag [0FH] associated with a sought after address concurrently with the mapper mapping the plurality of instructions into the predetermined instruction width format (see instruction length in col. 6, lines 40-52), see parallel decoders as mappers in fig. 5 and fig. 8); (c) selection circuit (select) one of the mapped instructions for decoding, wherein the parallel mapper is disposed in a pipelined computer system

upstream from the selection circuit, and wherein the parallel mapping, tag comparison, and selection are completed in a single pipeline stage (see the length decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52, see also prefetch, fetch decode and execute pipeline stages in fig. 2, see also the dual architecture pipeline in col. 2, lines 23-33).

Brennan did not expressly detail a decoder decoding the selected mapped instruction for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Claims 1-3,5,6,8,10-14,30,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) and Overkamp patent No. 7,069,420) in view of Lee (patent No. 6,442,674).

As per claims 1,30 Brennan taught a cache controller for use in a processor comprising (a) a plurality of mappers (see length decoders 35 in fig. 5) for receiving instructions of an instruction set, each mapper for mapping an instruction of said

instruction set to a predetermined instruction width format IPIWFI configuration (see length 00H and 0FH), wherein a plurality of mappers include at least one first mapper and at least one second mapper for receiving instructions for an instruction cache (see instruction cache 30 to the decoders 35 in fig. 4);

(b) multiplexer (see mux) for mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor. (b) receiving the PIWF configurations from the plurality of mappers (decoders) and selecting in response to a select signal [select] a desired one of the configurations (see also the length decoders 40 in fig 5) and in col. 6, lines 66-67, co. 7, lines 1-49, see also a plurality of parallel decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52)

Brennan did not expressly detail a decoder decoding the selected mapped instruction for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Brennan did not specifically show the mappers receiving instructions from a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation. Also the incorporation of the Lee teachings would have yielded predictable results.

As to the applicant remark that Brennan's determined instruction is not subsequently decoded (se applicant's remark in page 14 of the amendment on 03/26/08), Brennan already taught the length decoder 0 decodes the three selected bytes to generate a length value LO (see col. 7,lines 43-44). The length was a decoded result. On the other hand Overkamp taught subsequent decoding as discussed in the previous paragraph.

Furthermore, applicant might have argued that the length decoders of Brennan merely determined the length already mapped instructions, and did no have mapping of

their own. The examiner would like to point out that the length determined by the length decoders of Brennan was the mapping itself.

As to the applicant remark that Brennan independent claim 28, recites "mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration" Brennan taught mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see the length decoders 40 in fig 5 and col. 6, lines 66-67 and col. 7, lines 1-49), see also the plurality of parallel decoders in fig. 8, see the shifter 38 as a mux in col. 6, lines 40-52).

As to claim 32, Brennan taught at least: (a) parallel mapper maps the instruction held from a cache to the predetermined instruction width format (see how the prefetch of instructions from the cache 30 in fig. 4, see also fig. 4, 35, see fig. 5 for details of the decoder as a parallel mappers), (b) the tag comparator compares the tag associated with the instruction in a cache to the tag comparator compares the tag associated with the instruction in a cache to the tag of the sought after address concurently with the mapper mapping the instruction in the fill buffer into the predetermined instruction width instruction width format (see the instruction length in col. 6, lines 40-52), see parallel decoders as mappers in fig. 5, and fig. 8) and c) the selection circuit selects one of the mapped instructions or instruction held in a cache for decoding, wherein the parallel mapper is disposed in a pipelined computer system upstream from the selection circuit, and wherein the parallel mappling, tag comparison, and selection are completed in a single pipeline stage (see length decoders 40 in 35 in col. 6, lines 66-67, col. 7,lines 1-49, see also a plurality of parallel decoders in fig. 8 see the shifter 38 used as mux in

col. 6, lines 40-50, see also prefetch, fetch decode and execute pipeline stages in fig. 2, see also the dual architecure pipeline in col. 2 lines 23-33).

Brennan did not expressly detail a decoder decoding the selected mapped instruction for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Brennan did not specifically show his mappers receiving instruction from a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art

that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation. Also the incorporation of the Lee teachings would have yielded predictable results.

As to claim 2, Brennan taught a tag comparison (see detection on most significant bits with the 0FH in col. 6, lines 40-52) for the select signal [select]..

As to claim 3, Brennan taught comparing, for each instruction provided to one of the plurality of mappers, a tag (see most significant bits 0-2) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal (select) to cause said multiplexor to select said desired one of said PIWF configurations. As to claim 5, Brennan also (a) reading instructions of the instruction set from an instruction cache into a plurality of mappers (see fig. 5 decoders), wherein at least one of the instructions was read fro the instruction cache and at least one of the said instructions is read from the buffer, each instruction of the instruction set being read into a corresponding one of the plurality of mappers in preparation for mapping (see instruction cache 30 to the decoders 35 in fig. 4);(b) mapping each instruction of said instruction set to a corresponding PTWT configuration (see length 00H and 0FH); and (c) selecting a desired one of said PIWF configurations for decoding and execution by the processor (see also the length decoders 40 in 35 in col. 6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig. 8. see the shifter 38 used a mux in col. 6, lines 40-52).

Brennan did not specifically show his mappers receiving instruction from a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation. Also the incorporation of the Lee teachings would have yielded predictable results.

As to claim 6, Brennan also included comparing, for each instruction provided to one of the plurality of mappers, a tag (most significant bit) associated with an instruction of the instruction set to a desired tag (0FH) , wherein the desired one of the PIWF configurations is selected based on the comparison or detection (see selection).

As to claim 8, Brennan also included at least: (a) decoder (see either fig.4 instruction decoder or decoder 35), (b) cache for storing instructions (see cache 30 in fig. 4) ; and (c) a cache controller (not explicity characterized, but see how the prefetch of instructions form the cache 30 in fig. 4) for retrieving the instructions from the cache

and providing the instructions to a decoder (see fig. 4,35, fig. 5 for details of the decoder 35), comprising: a plurality of mappers including at least one first mapper for receiving instructions and at least one second mapper for receiving instructions from said instruction cache (see fig. 4, instruction cache), d) a multiplexor for selecting, in response to a selector signal, one of said PIWF configurations for decoding by the decoder (e.g, see col. 6, lines 40-52) and execution by the execution unit herein;(e) means for comparing, for each instruction provided to the multiplexor, a tag (see most significant bits) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal to cause said multiplexor to select said desired one of the configurations (see col. 6, lines 40-52), whereby performing instruction mapping substantially in parallel with tag comparison to improve processor performance (see parallel decoders as mappers in fig. 5 and fig. 8).

Brennan did not specifically show his mappers receiving instruction from a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main

memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation. Also the incorporation of the Lee teachings would have yielded predictable results.

As per claim 10, claim 10 is substantially the same as claim 1 and rejected under the same reasons as applied to claim 1. Claim 10 additionally recites the microprocessor cores embodied in software. Examiner holds that a microprocessor embodied in software is well known art (see pertinent reference (Painitkar et al. 5,539,680)., col. 1, lines 15-22, cited in this action, Palnitkar is not being used but it is ready to show examiner's position of well known art). As to the computer program product comprising a tangible readable storage medium having embodied thereon computer readable program code, see Brennan instruction cache in fig. 4. As to the first computer readable program code, see Brennan instruction cache in fig. 4. As to the first computer readable program code for providing a plurality of mappers see fig. 11, 120-130. As to the second computer readable program code, see Fig. 11 132 for issue to execution unit.

As to claim 11, see Brennan the selection in col. 6, lines 40-52.

As to claim 12 also included in a microprocessor core is embodied in hardware description language software (see pertinent reference (Palnitkar et al., 5,539,680) col. 1, lines 15-22), cited in this action Palnitkar is not being used but is ready to show examiner's position of well known art.

As to claims 13,14, examiner holds the microprocessor is embodied in Verilog hardware description language or VHDL had been known in the art (see the pertinent reference Palnitkar et al., 5539,680, col. 1, lines 15-22 cited in this action in paragraph, Palnitkar is not being used but it is read to show examiner's position of well known art).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-23,25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Brennan (patent No. 5,740,392).

As to claim 21,27, Brennan taught the invention substantially as claimed including decoding instructions in a processor comprising (a)mapping each of a plurality of instructions to a predetermined instruction width forma (PIWF) configuration (see length 00H and 0FH as the format configuration in fig. 5); (b) comparing in parallel with (a), tag for each of said plurality of instructions to an address (see detection of most significant bits with 0FH in col. 6, lines 40-52, most significant bits 0-2); (c) selecting, based on the comparison in the comparing, o'e of the PIWF configurations of the configuration to be decoded (see select signal [select]) and (d) decoding PIWF configuration selected for execution by processor core (see fig. 5 decoders, see also the length decoders 40 and 35 in col. 6, lines 66-67, col. 7,lines 1-49, see also parallel decoders in fig. 8).

As to claims 22,23,25,26, Brennan also included 16 bit and 32 bit (see fig. 2, Prefix (1-15) and 32 Bits).

Claim Rejections - 35 USC § 103

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) in view of Overkamp..

As to claim 28 Brennan taught a processor comprising a) mean for mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see configuration (see length 00H and 0FH); and c) multiplexer for receiving the PIWF configurations from means for mapping and for selecting, in response to a selector signal [select], desired one of the PIWF configurations for decoding and execution by the processor (see also the length decoders 40 in 35 col. 6, lines 66-67, col. 7,lines 1-49, see also a plurality of parallel decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52).

As to claim 28, Brennan taught mapping maps an instruction to a PIWF configuration (see the length decoders 40 in 35 in col. 6, lines 66-67, col. 7,lines 1-49, see also a plurality of parallel decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52).

Brennan did not expressly detail a decoder decoding the desired one of said PIWF configurations for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction configuration selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Claims 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) in view of Lee (patent No. 6,442,674).

As to the limitations of claims 24, limitations of claim 21 have been discussed in previous paragraph.

Brennan did not specifically show a fill buffer as claimed. Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions,

and in doing so, provided a movtivation. Also the incorporation of the Lee teachings would have yielded predictable results.

Claims 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) and Overkamp patent No. 7,069,420) in view of Lee (patent No. 6,442,674).

As to the limitations of claims 29, limitations of claim 28 have been discussed in previous paragraph.

Brennan did not expressly detail a decoder decoding the selected mapped instruction for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Brennan did not specifically show a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the

art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a movtivation. Also the incorporation of the Lee teachings would have yielded predictable results.

The change in scope of the amended claims has necessitated a new search.

Response to Arguments

Applicant's arguments, see amendment, filed 10/16/08, with respect to the rejection(s) of claim(s) under , 28,2,31,32 under 25 U.S.C. 102 and 1-3,5,6,8,10-14,24,29,30, under 35,U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Brennan, Overkamp and Lee respectively as detailed above. The rejections of claim 21-23,24-27 is maintained as set forth in the last office action.

As to claim 31 The Applicant argues that the parallel mapper is disposed upstream from the selection circuit. The Examiner contends that the disposition does not provide for limitations on the connection or order of processes or structure and therefore the disposition does not provide a difference between the Brennan reference and the claimed invention.

The Applicant argues with respect to claim 21 that the selecting based on the comparison in (b) , one of the PIWF configurations of (a) decoded and decoding the PIWF configuration selected in (c)(for execution by the processor core The Examiner contends that this limitation is taught by Brennan as detailed in the outstanding rejection above. As to the decoding the length Brennan taught the decoding operation that included outputting the length as detailed in the sections cited in the rejection above.

As to claim 28 Applicant argues that Brennan does not teach the newly added feature of "a decoder for decoding the desired one of said PIWF configurations for execution by the processor. Overkamp taught these limitations as detailed in the rejection above.

The Applicant argues the newly added limitation (in claim 8) of a plurality of mappers for mapping a plurality of instructions set to predetermined instruction width format (PIWF configurations and whereby the decoder decodes the desired format (PIWF) configurations for execution by the processor. This corresponding limitation newly added to the independent claims is detailed in the rejections above. Therefore claims 5, 10,31,32 are rejected for the same reasons.

Applicant acknowledges the cited prior art includes a filll buffer but alleges the fill buffer as described in the prior art does not include the claimed limitations. The Examiner contends that the fill buffer incorporation of the Lee fill buffer with the Brennan system provides for the claimed operation the fill buffers.

The rejection under 25 U.S.C. 101 hereby maintained and repeated above.

The applicant argues that the claims include a tangible computer readable storage medium. The Examiner however contends that the claims are read in light the specification and the specification does not separate the description of computer readable storage medium to a hardware device. The specification indicates that the computer usable (e.g.,readable) storage medium (e.g., medium configured to store) may be a transmission medium (or disposed on) a transmission medium (see paragraph 0054)and therefore is directed toward non-statutory subject matter.

As the objection to the specification corresponds the this problems stated 35 U.S.C. 101 rejection the objection to the specification is maintained an repeated above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hammond (patent No. 6,584,558) disclosed a system supporting different instruction sets (e.g., see abstract and figs. 8, 9).

O'Connor (patent No. 6,952,754) disclosed predecode system (e.g., see abstract).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

/Eric Coleman/
Primary Examiner, Art Unit 2183